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Current trends in processor design are pointing to deeper and wider pipelines and superscalar architectures. The efficient use of these resources requires *speculative execution*, a technique whereby the processor continues executing the predicted path of a branch before the branch condition is resolved. In this paper, we investigate the implications of speculative execution on instruction cache performance. We explore policies for managing instruction cache misses ranging from aggressive po ...
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Michael S. Meier , Kevan L. Miller , Donald P. Pazel , Josyula R. Rao , James R. Russell
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